Development of a Radiation Tolerant 2.0 V standard cell library using a commercial deep submicron CMOS technology for the LHC experiments.

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Abstract

A standard cell library was developed using a commercial 0.24 μm, 2.5 V CMOS technology. Radiation tolerant design techniques have been employed on the layout of the cells to achieve the total dose hardness levels required by LHC experiments. The library consists of digital core cell elements as well as a number of I/O pad cells. Additionally, it includes a pair of differential driver and receiver pads implementing the LVDS standard. The library cells have been fully characterised and the necessary descriptions to facilitate simulation have also been generated. The presented library features 5 times increase in speed accompanied by 26 times reduction in power consumption as well as an increase of 8 times in gate densities when compared to a currently available 0.8 μm CMOS technology. To prove the concept and to evaluate the radiation tolerance of the cells, a few demonstration circuits were implemented. The results of the radiation hardness tests are being reported.

1. INTRODUCTION

The collisions of TeV protons in the planned LHC collider at CERN will create a severe radiation environment inside the experimental equipment affecting the detector electronics [1]. For CMOS technologies the predominant damaging phenomena are threshold voltage shifts, transconductance and noise degradation and creation of leakage paths. Transient ionizing radiation effects like Single Event Upsets (SEU) and Single Event Latchup (SEL) are also of great concern.

With the use of thin gate oxides in deep submicron CMOS technologies the threshold voltage and the transconductance of the transistors are becoming less sensitive to radiation. Gate oxides with thickness in the order of 5 nm for gate lengths of about 0.24 μm become insensitive to charge trapping and interface state generation [2], [3]. The oxide trapped charge is roughly proportional to Tox^{-2} in this oxide thickness range, and its contribution to the total ionizing dose degradation becomes less important with advancing technology [4].

The hole trapping in lateral and field oxides, which are typically thick, is left as the main failure mechanism in submicron commercial technologies [5]. By introducing special layout techniques that aim to block all possible leakage paths that can be turned on due to the radiation these advanced technologies can become immune to irradiation.

The design of digital circuits of a significant size and complexity relies on the existence of a digital standard cell library and powerful CAE tools.

This study presents the work that has been performed in order to implement a radiation tolerant digital standard cell library on a commercial deep submicron CMOS technology. Radiation tolerant design techniques have been employed on the layout of the cells.

2. RADIATION TOLERANT LIBRARY

2.1 Description of the Technology

We have chosen to implement the digital library cells on a commercial 0.24μm, 2.5V CMOS technology. Irradiation tests that have been performed on this technology have demonstrated the hardness of the thin gate oxide [6]. The basic features of the selected technology are given in Table 1.

Table 1: Technology features

Minimum Lithography:	0.24 μm
Leff:	0.18 μm
VDD:	2.5 V
Gate Oxide Thickness:	5.0 nm (physical)
Process:	Twin well CMOS
Device Isolation:	Shallow Trench (STI)
Ti salicidation:	On n^+, p^+ polysilicon and diffusions
Interconnectivity:	2 to 5 metal layers

2.2 Radiation Tolerant Layout Techniques

Certain layout techniques have been proposed in order to increase the radiation tolerance of deep submicron technologies [6]. These techniques involve

- the use of "edgeless" or "enclosed" NMOS transistors that prevent the leakage current along the edges of the devices (edge leakage is eliminated since only thin oxide interfaces between source and drain) and
- the extended use of guardrings that isolate all n^+ diffusions that are at different potentials.

Figure 1 shows the use of these techniques in the layout design of an inverter and a 2-input NOR The PMOS devices are as well drawn using the enclosed geometry. The enclosed PMOS devices occupy less area

and at the same time offer smaller drain capacitance than the conventionally drawn devices. There is no significant role of the enclosed PMOS in the radiation tolerance of the cell.

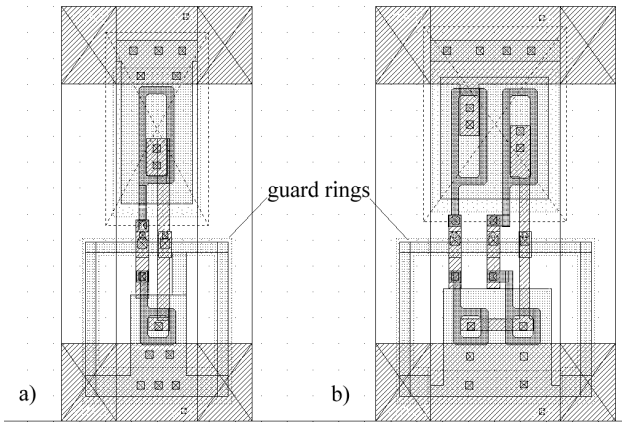

Figure 1. Layout patterns of a) a minimum size inverter and b) a 2-input NOR gate, as implemented in the Radiation Tolerant library.

2.3 Layout style

We have adopted a "traditional" layout design for the library leaf cell as depicted in Figure 2. Both power and ground rails lie outside the diffusion rows on the cell boundary. A p^+ guardring is placed around the NMOS diffusions that are connected at different potentials.

The power/ground rails (VDD/VSS) are routed in the first metal layer. Great effort has been spent to keep intracell interconnections on the first metal layer, leaving the rest of the metal layers for global routing. For that purpose the salicided polysilicon layer has been used as a local intracell interconnect. Since polysilicon cannot be allowed to cross the p^+ guardrings, as it would create a gap on them, this layer has been used only for horizontal routing. The first metal layer has been used for vertical intracell routing.

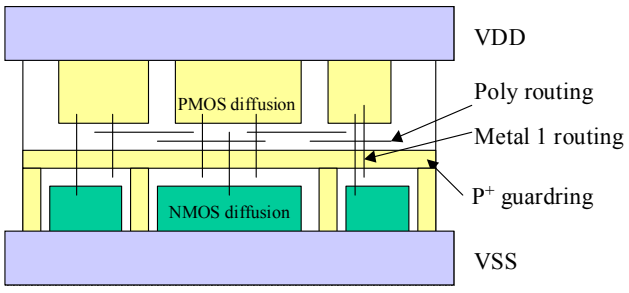

Figure 2. Cell layout style.

Obviously, a significant area penalty has been paid for the guardrings and the elimination of polysilicon interconnect over the guardrings. However, as it will be shown in *subsection 2.6* the area penalty is mitigated by the small feature size of the technology.

2.4 Library Contents

A set of digital standard cells consisting of core logic as well as I/O pads have been prepared and included in the library. In order to ease the library maintenance we decided to implement only a minimum set of cells that will enable the digital designing. The list of the standard cells that has been included in the presented library is shown in Table 2.

Table 2: List of digital library standard cells

Core Logic	
Inverter 1X Drive	Buffer X4 Drive
Inverter 2X Drive	Buffer X8 Drive
Inverter 3X Drive	NOR
Inverter 4X Drive	XNOR
2 Input NAND	2 Input NOR
3 Input NAND	2 Input NOR
4 Input NAND	2 Input NOR
2-Wide 2-In AND-OR	2-Wide 2-In OR-AND
2-Wide 3-In AND-OR	2-Wide 2-In OR-AND
3-Wide 2-In AND-OR	2-Wide 2-In OR-AND
Static D-F/F	Static D-F/F, Set
Static D-F/F, Reset	Static D-F/F, Set, Reset
Dynamic TSPC D-F/F	Static D-F/F, Scan
2-Input MUX	4-Input MUX
4-Bit Register, Clear	1-bit Adder
I/O Pads	
Input pad, CMOS	
Output, 8 mA drive	Output, 8 mA, slew rate
Output, 16 mA drive	Output, 16 mA, slew rate
Output, 20 mA drive	Output, 20 mA, slew rate
LVDS driver	LVDS receiver

The combinatorial core logic consists of simple gates like inverters and buffers with different driving capability, as well as NANDs, NORs and XNOR gates. More complex gates like AND-ORs, OR-ANDs and multiplexers have also been included.

Latches and flip/flops are the basic building blocks of sequential digital circuits and, to large extent, determine circuit speed and power dissipation. A static master/slave pseudostatic D-type Flip/Flop (D-F/F) has been included in the core logic of the presented library. A few other D-F/F cells based on this design that offer RESET, SET, and combined RESET-SET capabilities have also been included. A static 4-bit register with clear capability and a 1-bit adder have been included as well.

A dynamic True Single Phase Clock D-type Flip/Flop (TSPC D-F/F) has been designed according to the architecture proposed in [7] and included in the library. It requires only one clock signal and is positive edge triggered. This circuit is often the choice in pipelined datapaths and register files for signal processing circuits offering reduced power dissipation and less layout area when compared with the static D-F/F. Figure 3 and

Figure 4 presents the layout of both the static and the dynamic D-F/F for comparison.

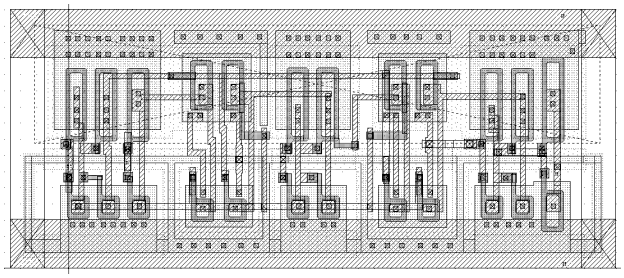

Figure 3. Layout pattern of the static D-F/F.

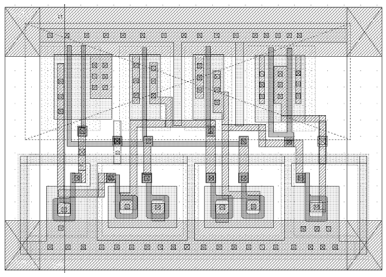

Figure 4. Layout pattern of the dynamic D-F/F.

A small set of I/O pads is included in the library. All pads offer ESD protection. Radiation Tolerant layout techniques have been also applied in the design of the ESD protection circuits. There are three types of output pads with different driving capability. Each type has a standard version and a version with a slew rate control output.

A set of "glue cells" have been developed to easy the design and enable the automated place & routing. These cells are: "cap cells" that closes the guardrings at both ends of the cell rows, corner cells for the chip power rings, power feedthrough cells etc.

2.5 CAE Tools

The availability of appropriate models, correct extraction rules and, in general powerful CAE tools to handle the deep submicron technologies, is a key issue in modern chip design. Special physical design verification rules have been added to check for inconsistencies in radiation tolerant designing (openings in the guardrings around n^+ diffusions etc). Special device extraction routines have been inserted in the extraction rules file that enable a more precise extraction of the size (W/L) of the enclosed geometry transistors. The library technology file has been set up with the necessary rules to allow generation of cell abstracts for the automated place & route.

Timing parameter extraction using SPICE simulations has been performed on the cells and models that enable the digital simulation have been developed.

2.6 Performance Characteristics

The gate delay of an inverter in the presented library is estimated from SPICE simulations to be 50 ps at 2.0 V (F.O.=1). This gives an improvement in speed of about 5 times when compared to a currently available 0.8 μm technology.

The estimated power consumption in the presented library is estimated to be 0.15 μW/MHz/gate (F.O.=1), which is 26 times lower than what is achieved in a 0.8 μm technology.

In order to reduce further the power consumption, as the intrinsic speed of the technology is high, we propose to use the library cells at 2.0 V rather than 2.5V, which is the nominal operating voltage of the technology.

Table 3 shows the estimated propagation delay (Tpd) and the associated power dissipation of a simple inverter (F.O.=1) cell at 2.5 V and 2.0 V. The speed of the technology even after a reduction of 25% will still overwhelm the requirements for the circuit operation in the LHC environment. At the same time the power dissipation is almost halved relaxing the power budget constrains for the detectors front-end electronics. All the cells in the presented library have being characterised at a typical operating voltage of 2.0 V.

Table 3: Speed/Power trade-off at reduced VDD.

	2.5 V	**2.0 V**	
Tpd	36 ps	48 ps	-25 %
Power	0.24 μW/MHz	0.14 μW/MHz	-42 %

The penalty that the radiation tolerant techniques introduce in the library cells is estimated to be about 70%. For comparison a sample of a few digital cells were drawn, on the selected deep submicron technology, using standard and radiation tolerant layout techniques. The area of the layout of each cell as well as the associated penalty in the area can be seen on Table 4. The comparison shows also that more complex cells exhibit higher area penalty.

Table 4: Area penalty due to radiation tolerant design.

	Standard	**Rad-Tol**	**Penalty**
Inverter	33.6 μm^2	50.9 μm^2	34 %
2-in NAND	46.0 μm^2	119.0 μm^2	61 %
2-in NOR	47.8 μm^2	80.0 μm^2	41 %
Static D-F/F	153.0 μm^2	533.1 μm^2	71 %
Static D-F/F SR	188.1 μm^2	572.0 μm^2	75 %

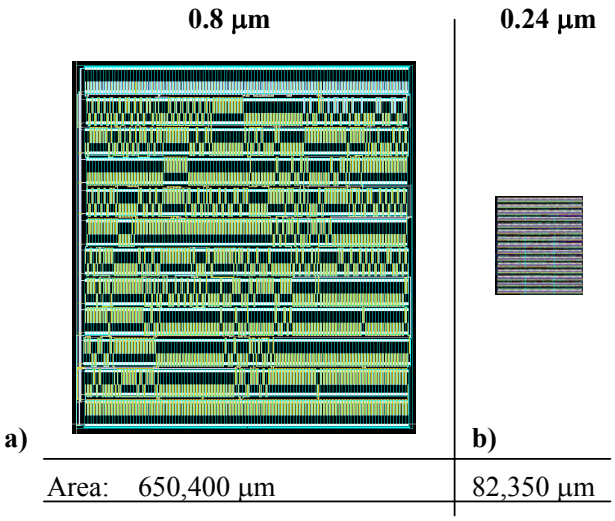

Figure 5. Layout of a ring oscillator consisting of a 1,280 inverters drawn on a) a typical 0.8 µm technology using standard cells and b) on the 0.24 µm technology using the radiation tolerant standard cell library.

Despite the area overhead, the gate density offered by the presented library is still 8 times higher when compared to a 0.8 µm standard cell technology. Figure 5 shows the layout of a ring oscillator consisting of 1,280 minimum size inverter cells drawn on a 0.8 µm standard cell technology and on the 0.24 µm technology using the radiation tolerant standard cell library. Both designs were routed using 2 metal layers. The design in the 0.24 µm technology was found to be 7.9 times smaller than the one in 0.8 µm. The fact that the presented library features up to 5 levels of metal for wiring purposes, presents an advantage for the high density designs.

3. DEMONSTRATOR CHIP

3.1 Test Chip

In order to evaluate the radiation tolerance of some of the designed standard cells as well as to demonstrate the functionality of the developed design kit we have designed a few digital circuits that were fabricated on the referring technology. The circuits were:

- a *Ring Oscillator* consisting of 1000+1 minimum size inverters,
- a *Static Shift Register* consisting of 2,048 static D-F/F cells,
- a *Dynamic Shift Register* consisting of 1,024 TSPC D-F/F cells,
- an *SEU Tolerant Static Shift Register* consisting of 2,048 specially designed D-F/F cells and
- a pair of LVDS receiver and driver.

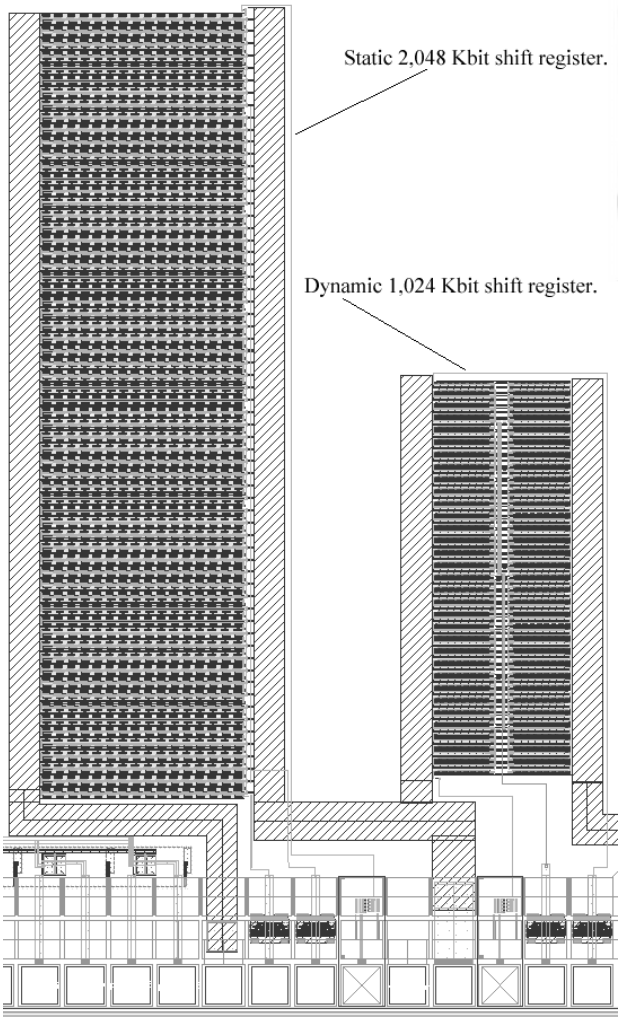

Figure 6. Part of the test chip showing the static and the dynamic shift registers.

Figure 6 shows part of the layout of the submitted chip presenting the layout design of the static and the dynamic shift registers.

All the implemented circuits were tested and found to be functional.

3.2 LVDS receiver and driver

The receiver was designed to operate at a nominal power supply of 2.0 V, however, it was possible to operate it successfully at power supply voltages between 1.5 V and 2.5 V. Since the allowed common mode range for an LVDS signal in the input of an LVDS receiver is 0.2 V to 2.2 V and the receiver was designed for a 2.0 V nominal power supply, its input stage was designed as a true rail-to-rail amplifier. The tests showed that the receiver can be operated with common mode voltages between 0 V and the power supply voltage. Tests were carried out for frequencies up to 120 MHz. The receiver displays a nominal delay of 830 ps for an input

differential signal of 300 mV amplitude. Figure 7 shows an eye diagram measurement of the receiver.

The LVDS driver was also tested but it was verified that, due to a "missing connection", only one of the differential outputs was operational. This prevented further testing and qualification of the driver and required the use of a commercial LVDS driver to test the receiver. The "missing connection" was due to an inconsistency in the technology file used to verify the circuit before fabrication. This verification problem has now been identified and corrected.

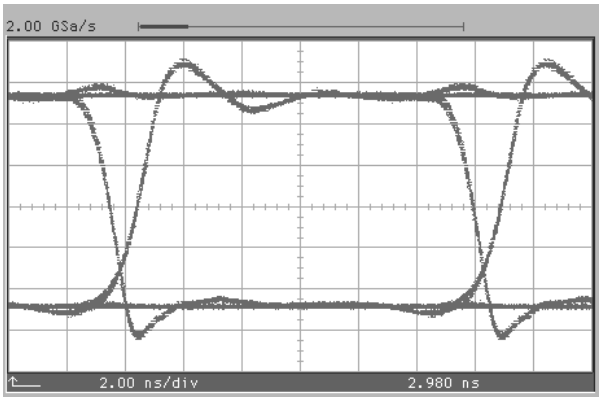

Figure 7. Eye diagram of the LVDS receiver.

4. RADIATION HARDNESS TESTS

Hereafter we present the results of total dose irradiation tests performed on the ring oscillator and the LVDS receiver. Results of total dose irradiation tests performed on the three shift registers are presented separately [8]. The three shift registers were also studied for Single Event Upset (SEU) and Single Event Latchup (SEL) effects. The results of these studies are also presented in [8].

4.1 Ring Oscillator

For the total dose irradiation tests on the ring oscillator we have used a 10 KeV X-ray machine. The dose rate was 29 Krad/min. The irradiation was performed at room temperature having the circuits under bias at 2.0 V. A step irradiation was performed at 1, 3, 5, 10 and 30 Mrad. The operation frequency and the power consumption of the ring oscillator were measured at every irradiation step. After the total dose of 30 Mrad the device under test was left for 24 hours under bias at room temperature for annealing and then another set of measurements was performed. After the 24 hours annealing period the device was kept under bias for a weak in an oven at 100^{o}C and measured again. This procedure complies with the ESA qualification procedure described in [9].

Figure 8 shows the inverter propagation delay (Tpd) as a function of the power supply (VDD) for different irradiation steps. The propagation delay was found to be 59.8 ps before irradiation and at 2.0 V, which is in good agreement with the estimated value from SPICE simulations. After 30 Mrad of total ionizing dose we have measured an increase in the propagation delay of 5.2 %. This increase matches with the measured degradation in the device mobility as presented on [8]. Figure 9 summarises the degradation of the propagation delay for different irradiation levels. The ring oscillator was fully functional down to power supply voltage of 1.0 V at all irradiation levels. After 1 week annealing the propagation delay did not show any further degradation.

Figure 10 shows the measured power delay product (Pw) of the inverter as a function of the power supply voltage (VDD). The Pw before irradiation and at 2.0 V was found to be 0.15 μW/MHz which is in very good agreement with the estimated value from SPICE simulations. The stability of the power delay product curve indicates that there is no increase in the leakage currents associated with the total dose radiation. This result demonstrates the effectiveness of the radiation tolerant layout techniques.

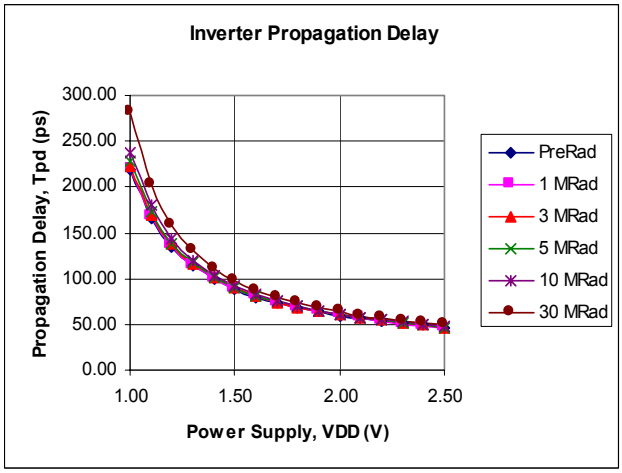

Figure 8. Inverter propagation delay (Tpd) as a function of the power supply voltage (VDD) at different irradiation levels.

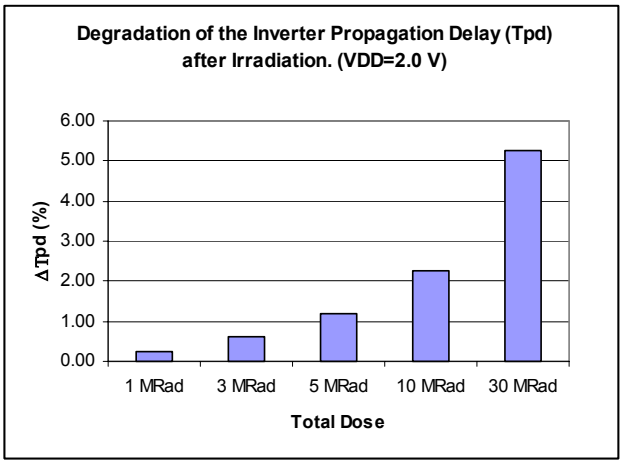

Figure 9. Degradation of the inverter propagation delay (Tpd) at different irradiation levels, at 2.0 V power supply voltage.

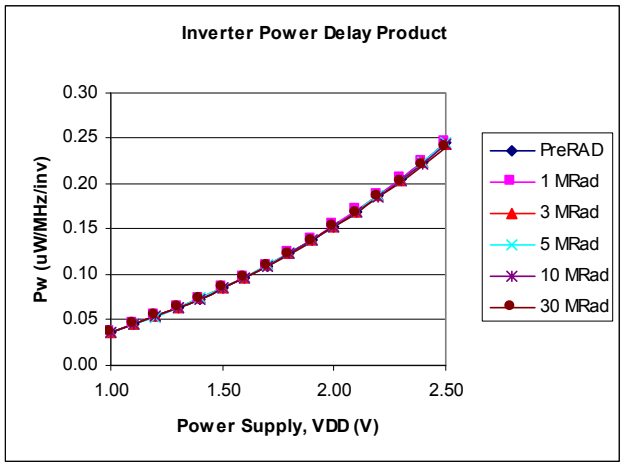

Figure 10. Inverter power delay product (Pw) as a function of the power supply voltage (VDD) at different irradiation levels.

4.2 LVDS receiver

The LVDS receiver was submitted to X-ray radiation under bias and at the ambient temperature at a dose rate of 16.2 Krad/min. The irradiation tests were made in two steps: one up to a total dose of 1 Mrad and the other up to 10 Mrad. In both cases the receiver was tested after irradiation with the performance showing no observable degradation after the 1 and the 10 Mrad irradiation steps.

5. FURTHER WORK

To fully utilise the presented digital standard cell library a proper interface with a logic synthesis CAE tool is necessary.

Interconnect width and spacing are also scaled down with device scaling making the 3D fringing fields significant in the multi-level interconnect capacitances. A tool that will be able to extract interconnect parameters (RC) accurately is of great importance. Especially for full chip global critical paths, the interconnect modelling has to be accurate. Conventional parameter extraction tools from commercial vendors use 2D approximation for 3D capacitances. 3D fringing fields are significant in the multi-level interconnect capacitances.

Another fabrication test run will be required in order to extract the timing parameters for the designed digital cells from measurements leading to more precise timing models.

6. CONCLUSIONS

We have developed a radiation tolerant 2.0 V standard cell library using a commercial 0.24 μm CMOS technology. The selected technology was found to be natively radiation resistant mainly due to the utilisation of thin gate oxide and possibly by the utilisation of STI between the devices. With the introduction of special layout techniques in the cell design we have increased further its radiation resistance leading to total dose radiation levels which are compatible with LHC design requirements.

Moreover, the use of an advanced deep submicron technology presents many advantages in terms of speed power and area utilisation over currently available technologies.

We have shown that despite the area overhead implied by the radiation tolerant layout techniques, the presented library is still superior in gate density of about 8 times when compared to a 0.8 μm technology.

We have developed a design kit to support the standard cell library that offers digital simulation capabilities as well as layout extraction and verification. The functionality of the design kit was tested and demonstrated with the implementation of a number of digital circuits in a test chip. The circuits consisted of a ring oscillator, a static shift register, a dynamic shift register and a novel design of a static shift register that features reduced rate of single event upsets. The test chip was fabricated and the circuits were tested and found to be fully operational.

The radiation performance of the standard cell library has been demonstrated with the submission of the ring oscillator in total dose irradiation tests. Only 5.2 % degradation in speed was measured after 30 Mrad of total dose, while there has not been any leakage current turn-on.

Differential signalling transmission will find its use in clock distribution on the detectors front-end electronics, where good timing information, low power and low noise emission is of concern. The availability of a pair of differential I/O pads that follows the LVDS signalling standard is of an advantage for the presented library. We have demonstrated the functionality of the differential receiver pad. The tests showed that the receiver is able to operate with a common mode from rail-to-rail (0.0 V to 2.0 V) at maximum frequency of 120 MHz.

7. REFERENCES

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