Configurable Dual Port SRAM Module

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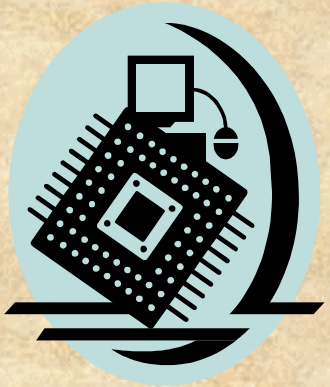
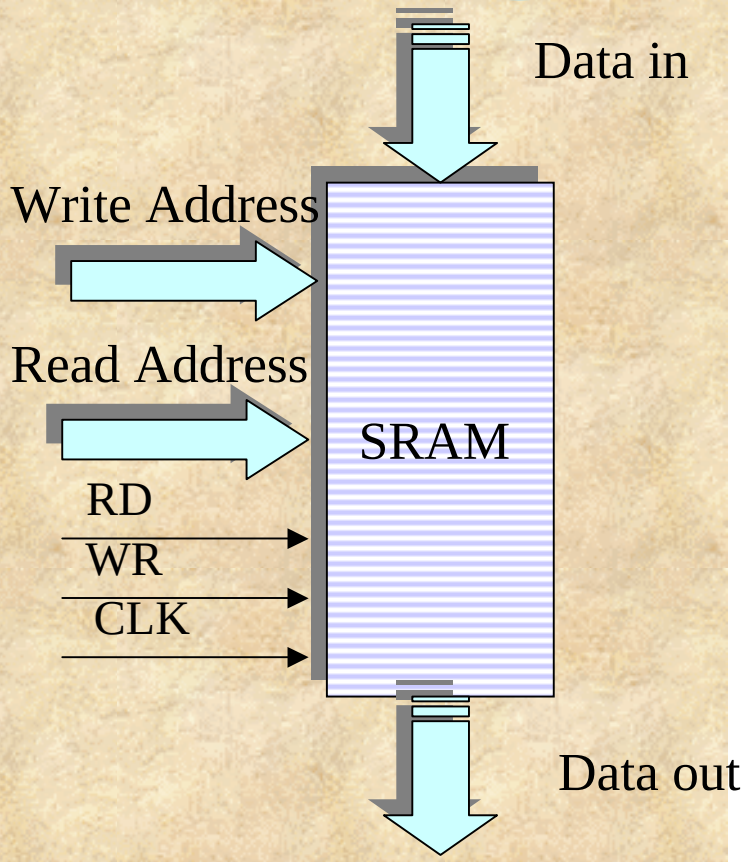
SRAM Features

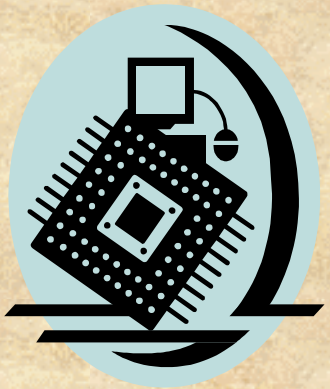


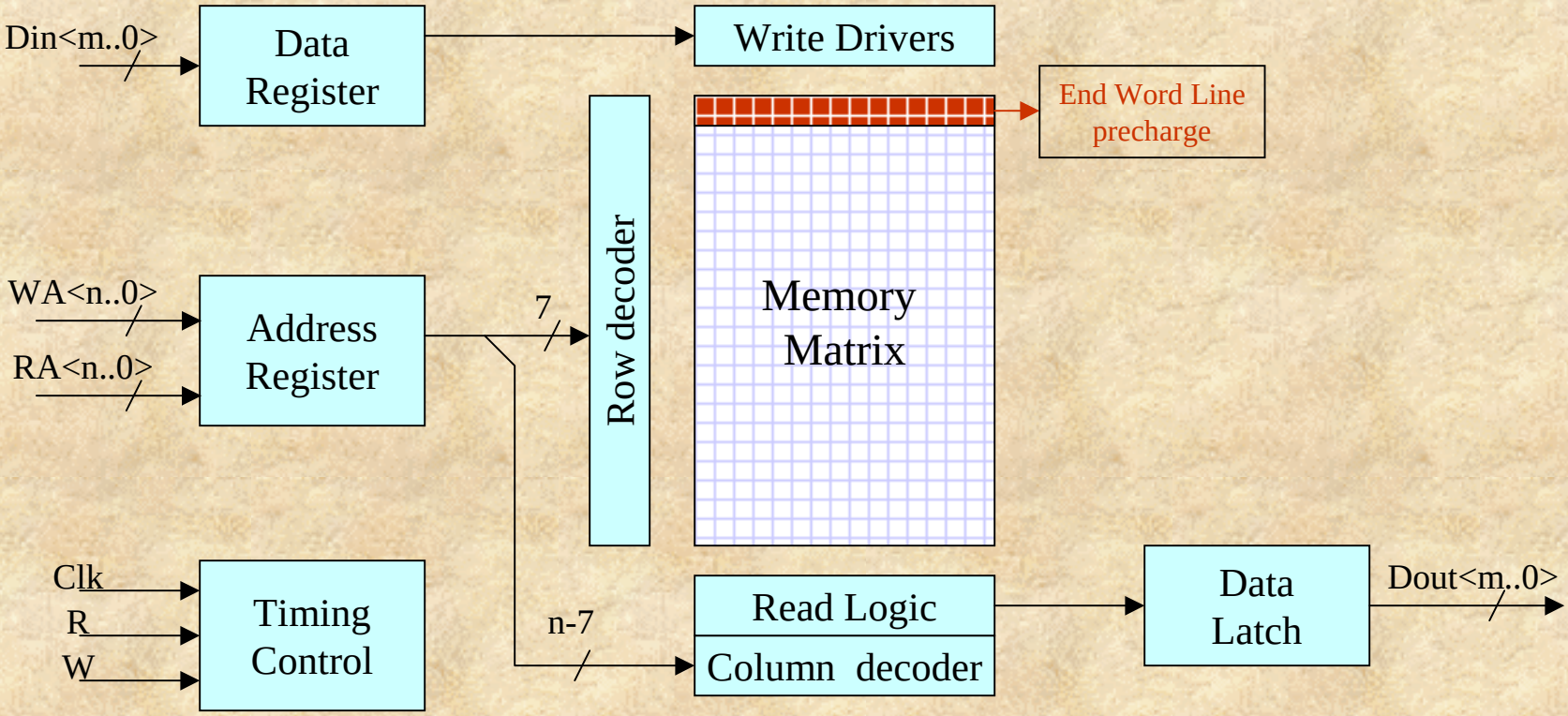
- **Synchronous *pseudo* Dual Port Operation**
- **Self timed logic**
- **Registered Inputs, Latched outputs**
- **Radiation Tolerant Design**
- **Typical Operation freq.: 40MHz**
- **Configurable Macro design**
- **Data bus width: (n x 9)bits**
- **Data arrangement: 8 + 1 parity**
- **Memory Size: up to 4K words**



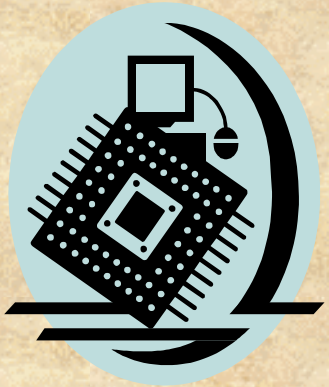
Dual Port SRAM

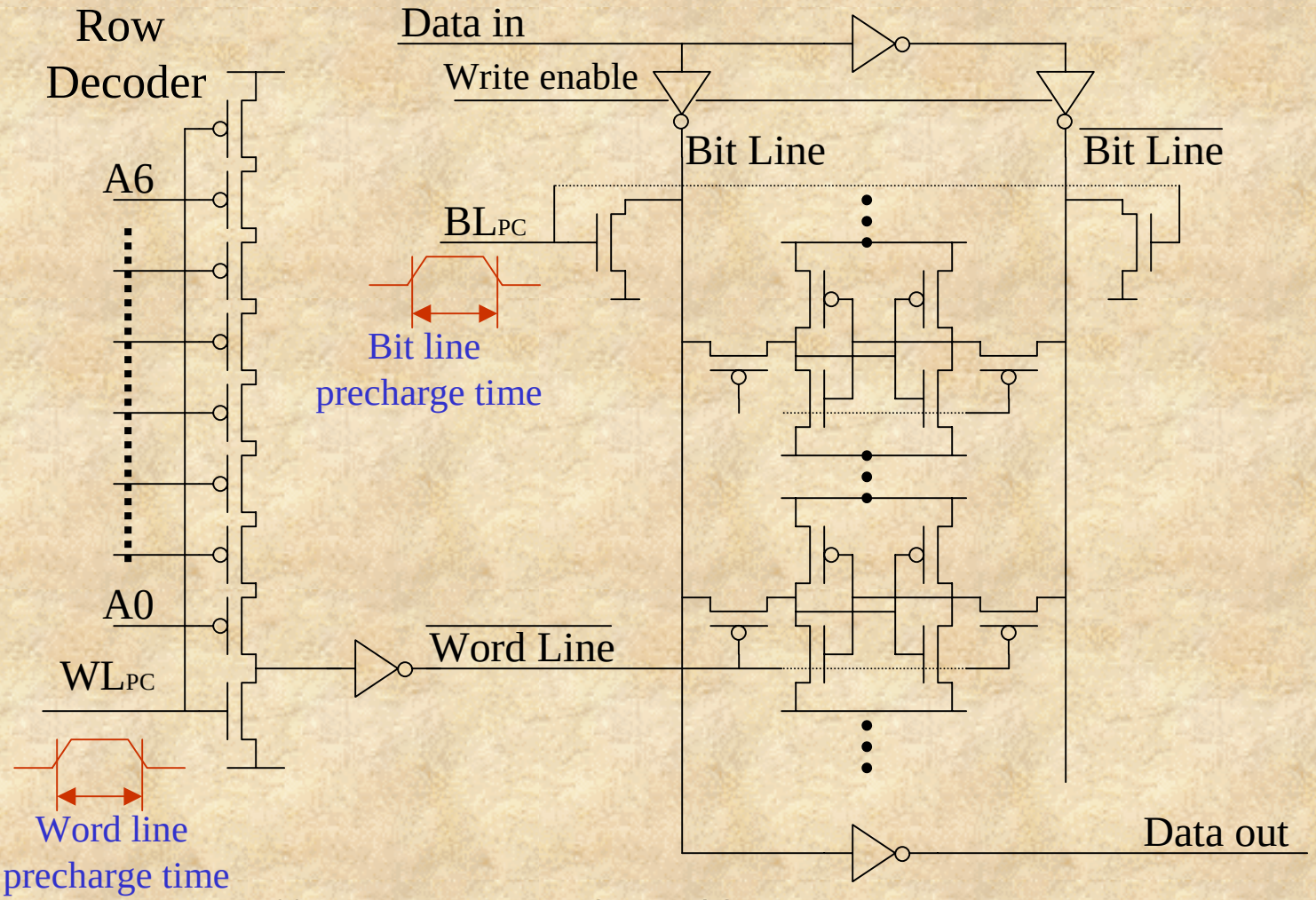
block diagram



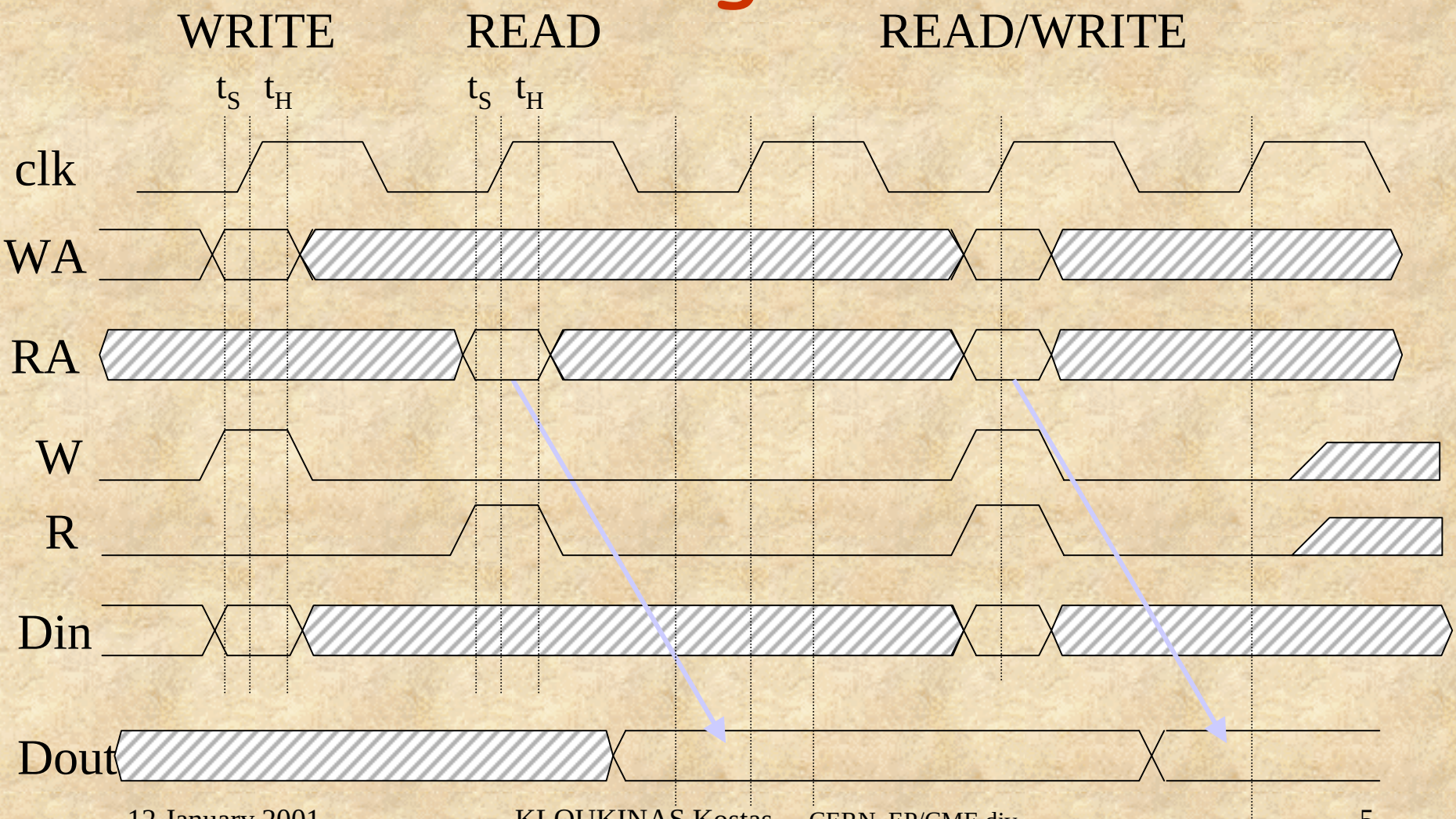


SRAM Design in 0.25μ

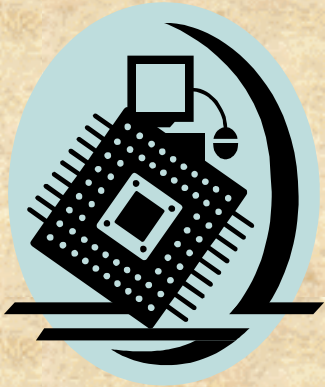


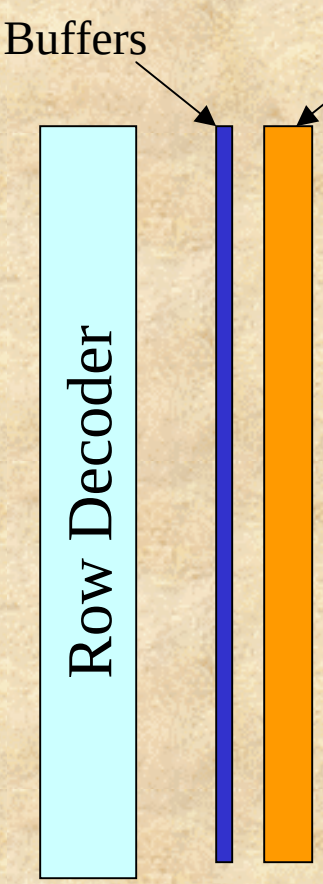


SRAM Interface Timing Diagram



Basic Layout Blocks





Input Data Registers

Address Registers

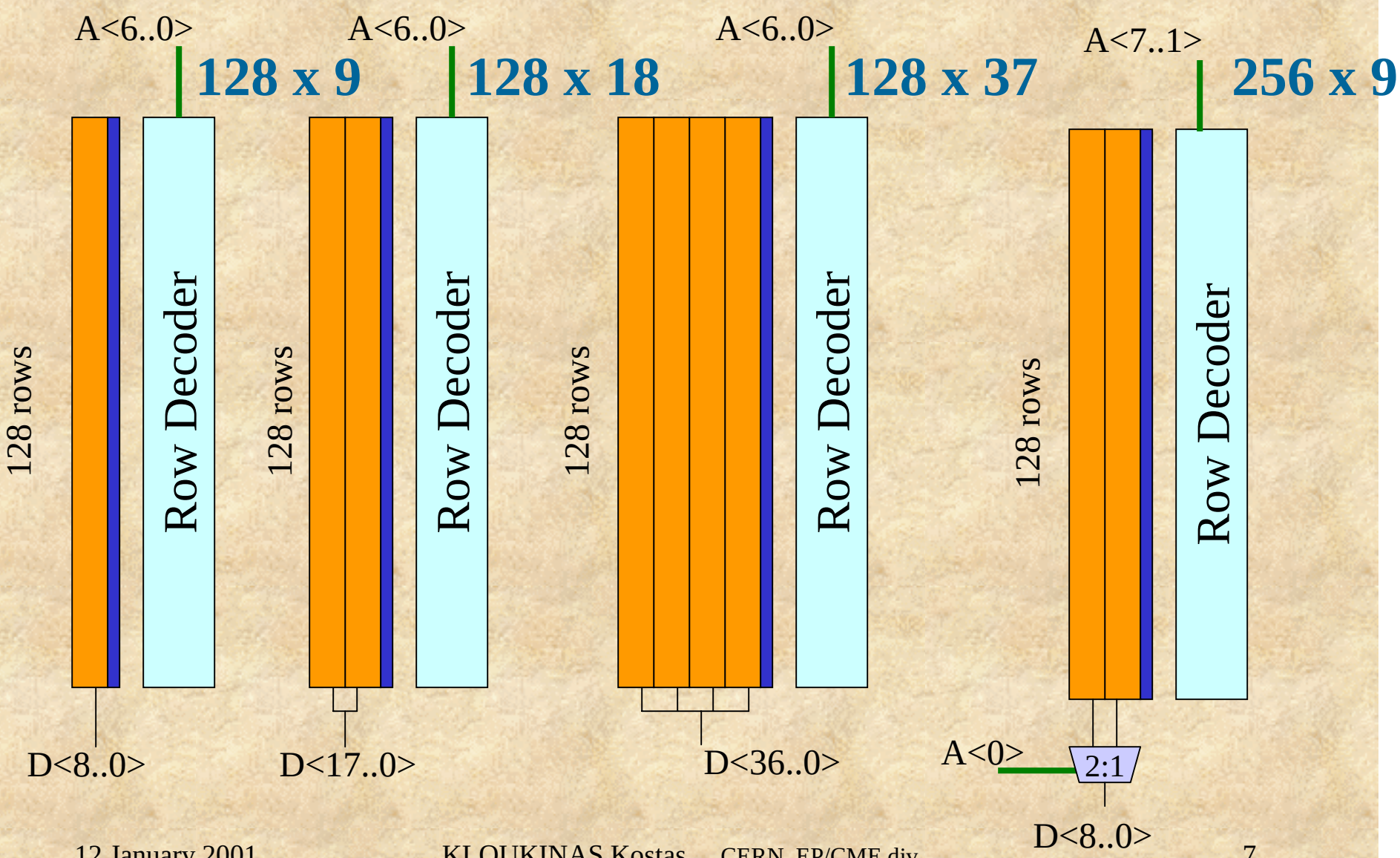
Timing logic

Column Decoder

Output Data Mux

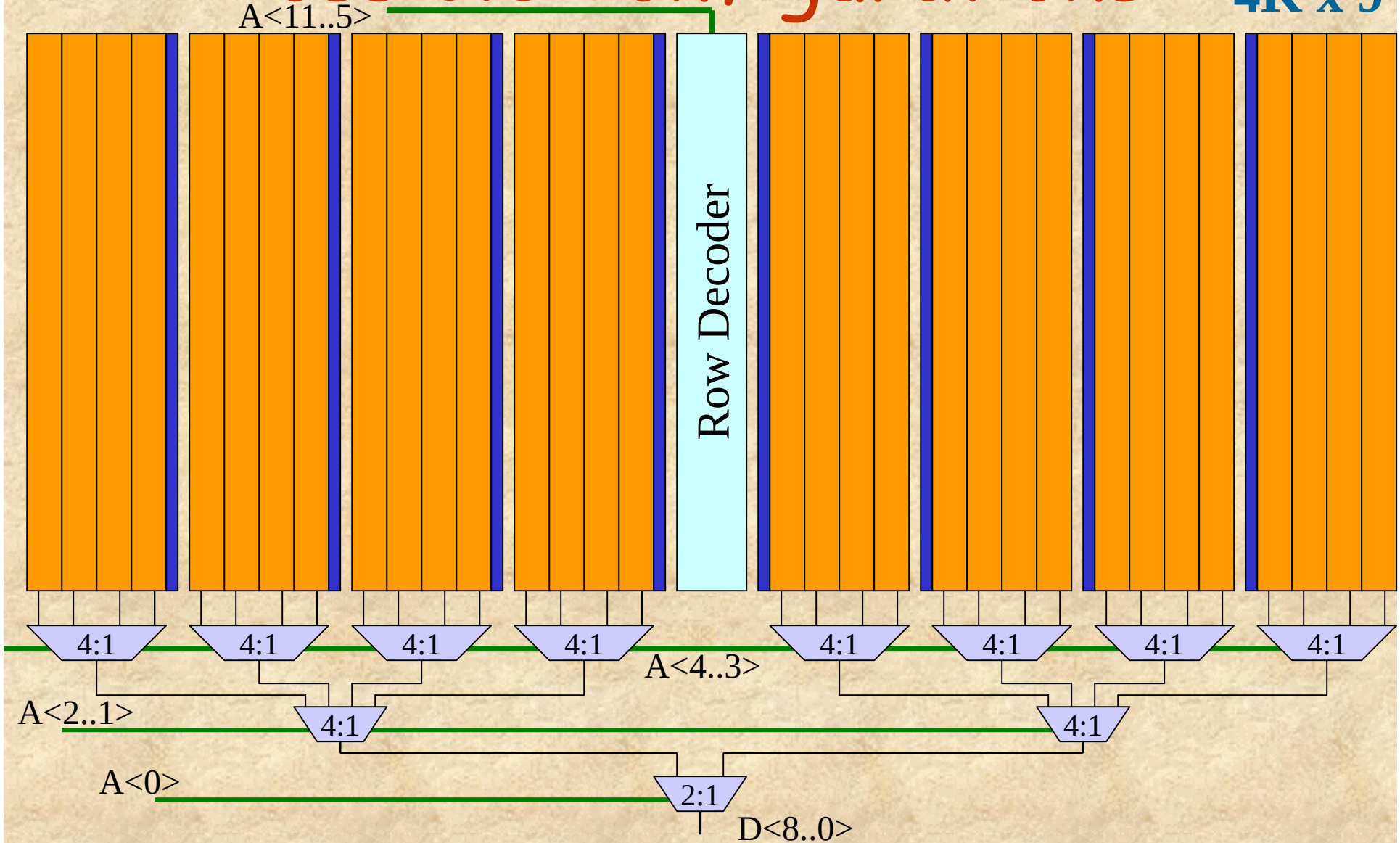
Output Data Latches

Possible Configurations



Possible Configurations

4K x 9



Submitted SRAM Chip

- **Configuration: 1Kx9 bit**
- **Size: ~560μm x 1,300μm**
- **Area: ~0.73mm^2**
- **Submitted: Oct. 2000.**