Development of a Radiation Tolerant 2.0 V standard cell library using a commercial deep submicron CMOS technology for the LHC experiments.

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Introduction

A standard cell library was developed using a commercial 0.24 µm, 2.5 V CMOS technology. Radiation tolerant design techniques have been employed on layout of the cells to achieve the total dose hardness levels required by LHC experiments. To prove the concept and to evaluate the radiation tolerance of the cells, a few demonstration circuits were implemented. The results of the radiation hardness tests are being reported.

Technology

Lithography (min):	0.24 µm
L_{eff}:	0.12 µm
V_{dd}:	2.5 V
Gate Oxide Thickness:	5.0 nm
Process:	Twin well CMOS
Device Isolation:	Shallow Trench (STI)
Ti salicidation:	On N^+, P^+ polysilicon and diffusions
Interconnectivity:	2 to 5 metal layers

Library Design Kit

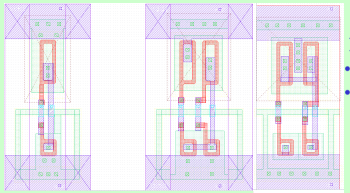
Radiation Tolerant library design kit offers:

- Physical Verification (*Rad-Tol design checks*)
- Device Extraction (*enclosed devices*)
- Digital Simulation (*timing models*)
- Placing & Routing

Cell List

Core Logic	
Inverter 1X Drive	Buffer X4 Drive
Inverter 2X Drive	Buffer X8 Drive
Inverter 3X Drive	NOR
Inverter 4X Drive	XNOR
2 Input NAND	2 Input NOR
3 Input NAND	2 Input NOR
4 Input NAND	2 Input NOR
2-Wide 2-In AND-OR	2-Wide 2-In OR-AND
2-Wide 3-In AND-OR	2-Wide 2-In OR-AND
3-Wide 2-In AND-OR	2-Wide 2-In OR-AND
Static D-F/F	Static D-F/F, Set
Static D-F/F, Reset	Static D-F/E, Set, Reset
Dynamic TSPC D-F/F	Static D-F/E, Scan
2-Input MUX	4-Input MUX
4-Bit Register, Clear	1-bit Adder
I/O Pads	
Input pad, CMOS	
Output, 8 mA drive	Output, 8 mA, slew rate
Output, 16 mA drive	Output, 16 mA, slew rate
Output, 20 mA drive	Output, 20 mA, slew rate
LVDS driver	LVDS receiver

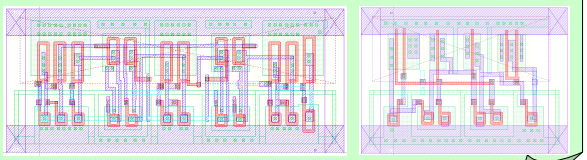
Radiation Tolerant Layout



Radiation Tolerant design :

- enclosed NMOS transistors
- guardrings that isolate all n^+ diffusions at different potentials

1X inverter **2-in NOR** **2-in NAND**



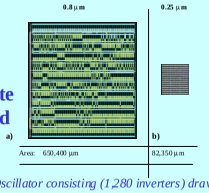
Static D-F/F **Dynamic TSPC D-F/F**

Performance

- Inverter propagation delay: **60 ps**
- Power delay product: **0.15 µW/MHz/gate**
- Radiation Hardness tested up to: **30Mrad**

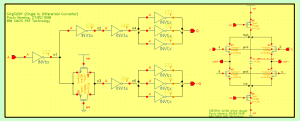
Compared to a 0.8 µm technology

- SPEED: 5X increase in speed
- POWER: 26X reduction in
- AREA: 8X increase in gate density

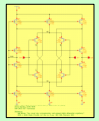


Ring Oscillator consisting (1,280 inverters) drawn on a) a typical 0.8 µm technology using standard cells b) on the 0.24 µm technology using the radiation tolerant standard cell library.

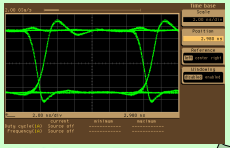
LVDS I/O pads



LVDS Driver



LVDS Receiver

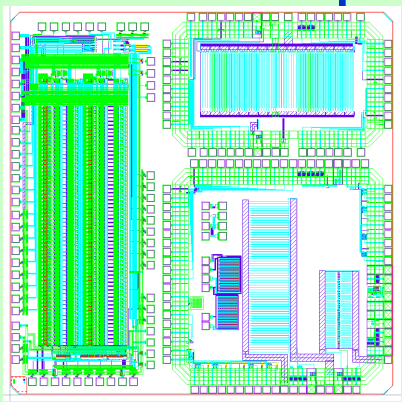


LVDS Receiver Eye Diagram

LVDS Receiver measured params:

- Power Supply: 2.0 V
- Common mode: 0.0 V - 2.0 V
- Max frequency: 120MHz
- Tpd (typ): 830 ps

Submitted Chip

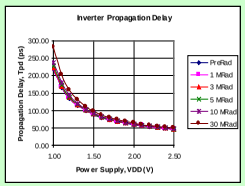


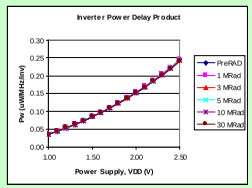
Implemented Digital Circuits:

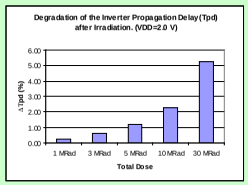
- Ring Oscillator
- Static Shift Register (2,048 D-F/F)
- Dynamic Shift Register (1,028 TSPC D-F/F)
- SEU tolerant Static Shift Register (2,048 F/F)
- Standard I/O pads & LVDS I/O pads

Radiation Tests

Test circuit: Ring Oscillator (1001 inverters).
Dose rate: 29Krad/min
Test conditions: under bias (2.0 V) @ 25ºC







Results:

- **No leakage current turn on**
- **Propagation delay degradation:**
  ΔTpd = 5.2 % @ 30 Mrad